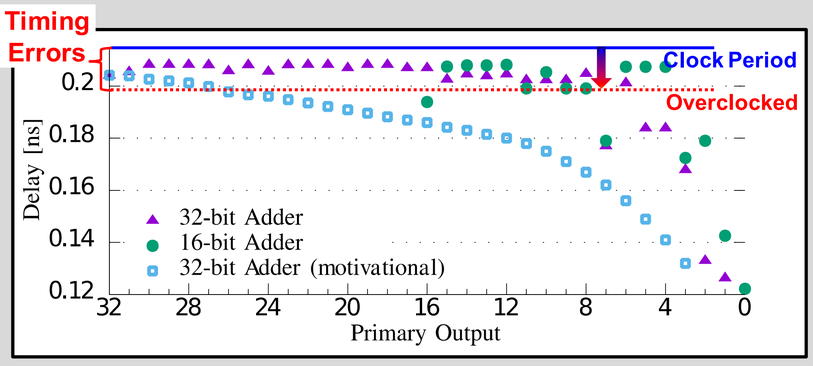
Karlsruhe Institute of Technology

Chair for Embedded Systems

SlackHammer: Logic Synthesis for Graceful Errors Under Frequency Scaling

Tanfer Alan and Jörg Henkel

Circuit Level Timing Speculation

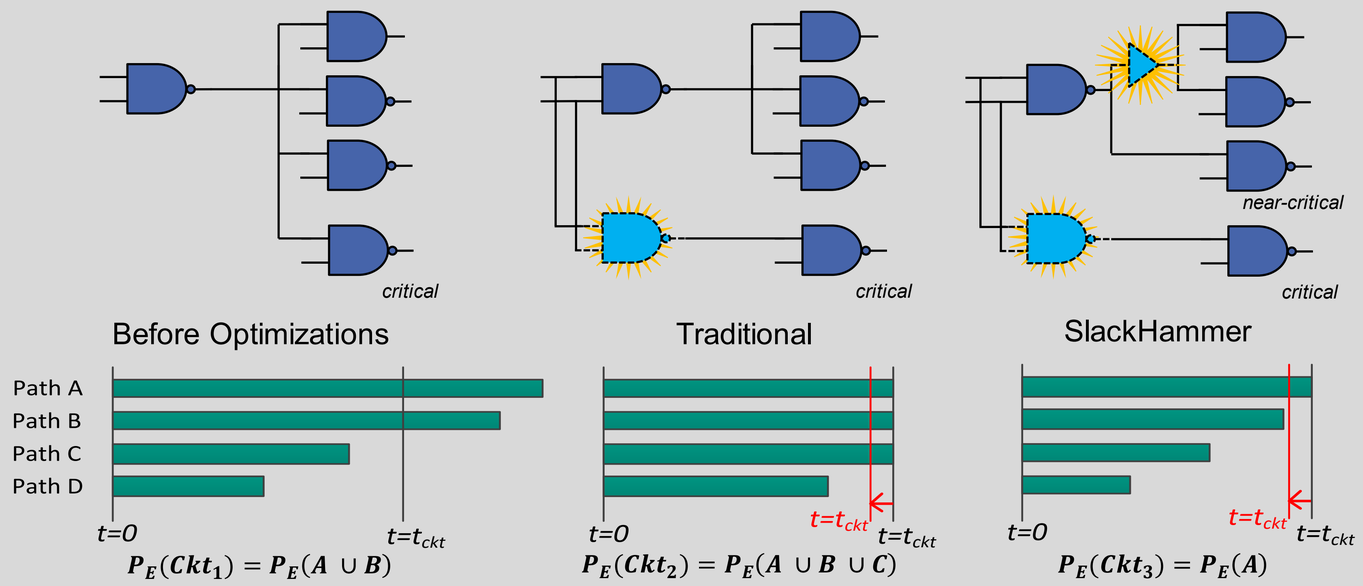


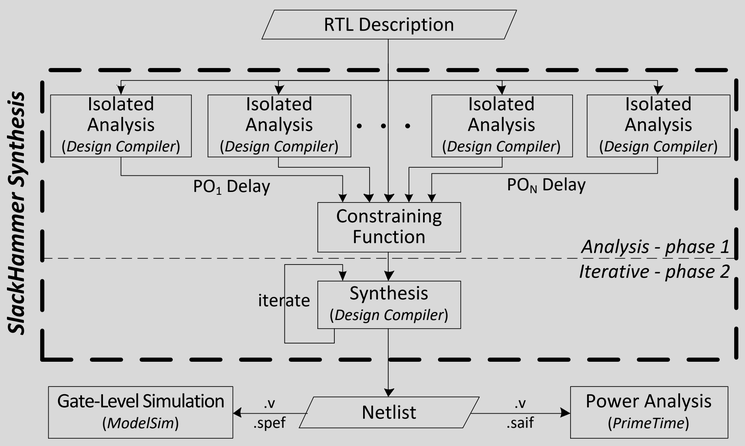
Idea
Most input combinations do not invoke the critical path and can be accomplished in a shorter time or lower voltage.

Observation
Synthesis algorithms result in circuits that contain a large number of near-critical paths.
→ Under aggressive voltage or frequency scaling either no error occurs, or a very large number of paths fail at the same time.
→ Timing speculation benefits are limited.

Motivation
1. Reduce the number of near-critical paths
2. Enable graceful errors under frequency scaling
   → increase the performance

Proposed: Non Critical Path Optimizations





Methodology
Set tightest, successful delay constraints for each primary output in 2 phases:
1) Analysis
   - Identify non-critical paths
   - Asses the delay improvement margin
   - Set initial delay constraints
2) Iterative constraining
   - Relax the worst violator constraints until synthesis successfully finishes

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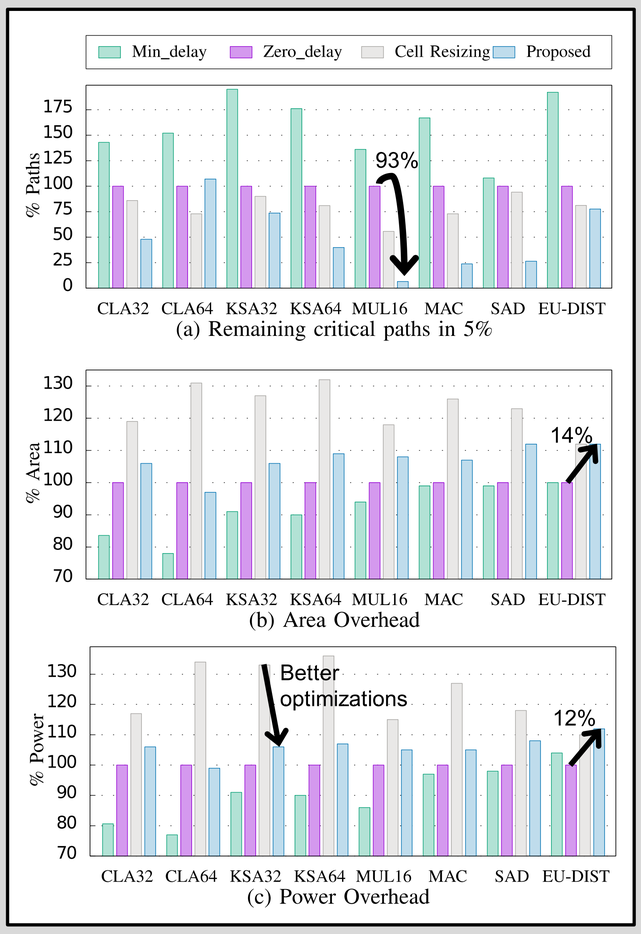
constraint[s] = constraint[s]+ δ
```

Delay Reductions



Results
The number of near-critical paths are reduced by up to **93%**.

Better optimizations: area and power overheads are significantly less than the state-of-the-art, post-synthesis cell resizing method [1].

Limitations
Inherits synthesis heuristics

Design time overhead **15x – 623x** depending on:
- Number of primary outputs
- step size (δ) in iteration phase

Delay Distribution Comparison
Most primary output delays can be reduced lower than what traditional synthesis methods produce.

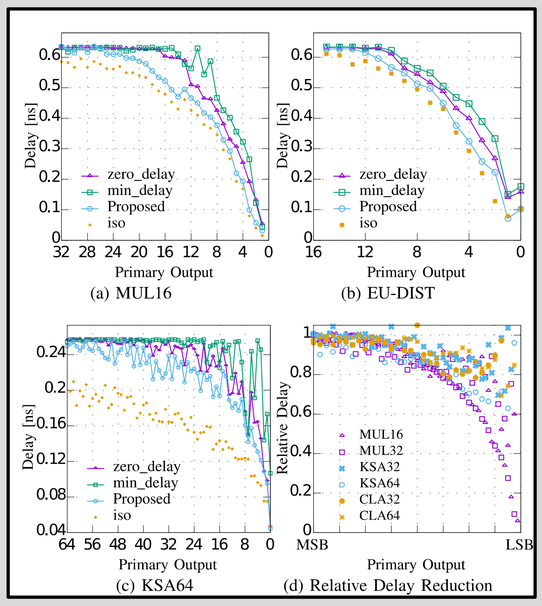


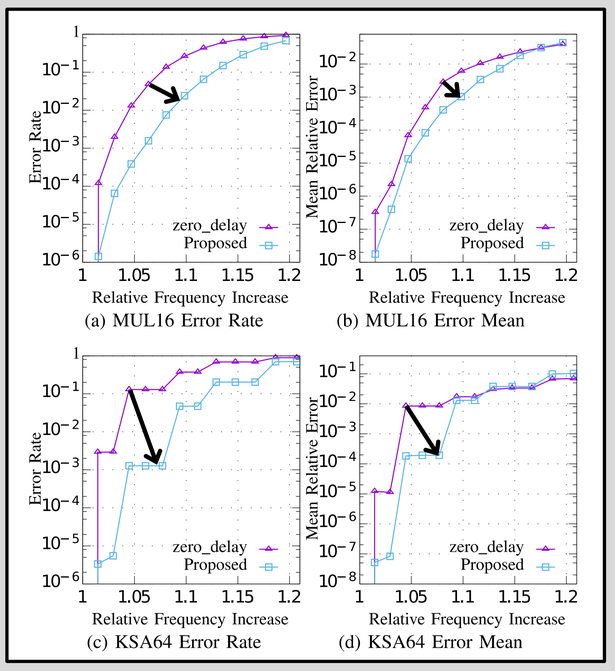
TABLE I: Circuits used in experiments

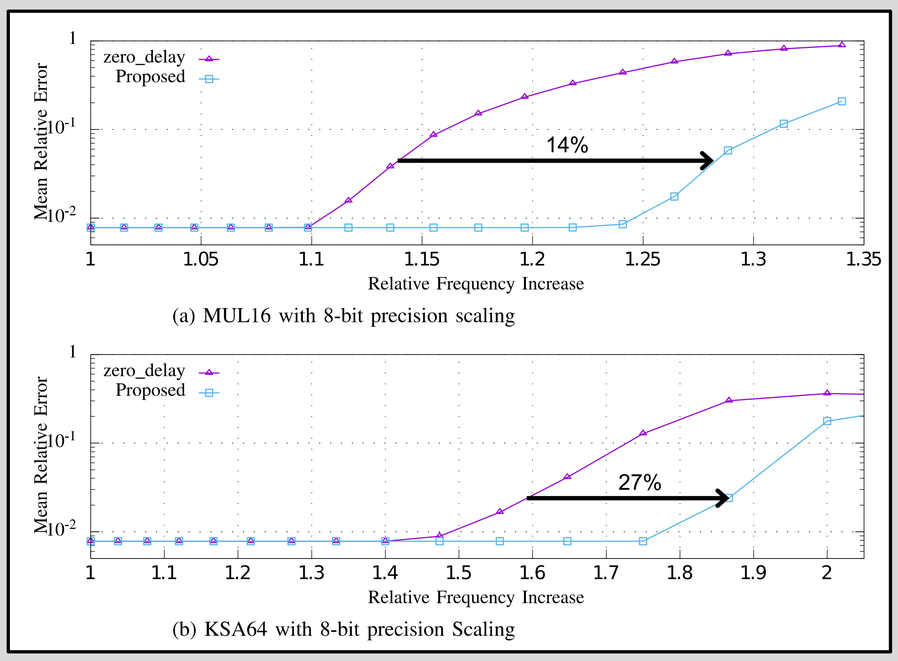
Name	Function	Bitwidth	I/O
CLA32	Carry Look-ahead Adder	32	64/33
CLA 64		64	128/65
KSA32	Kogge-Stone Adder	32	64/33
KSA64		64	128/65
MUL16	Multiplier	16	32/32
MAC	Multiply and Accumulate	8	48/33
SAD	Sum of Absolute Differences	8	48/33
EU-DIST	Euclidian Distance (without square-root)	8	16/16

Error Characterizations

Accuracy – Frequency Tradeoff
Reductions in error rate and error magnitude can be achieved with proposed non critical path optimizations.

Cross-Layer Effectiveness
SlackHammer circuits start producing errors later when frequency is overscaled.





[1] Kahng, Andrew B., et al. "Slack redistribution for graceful degradation under voltage overscaling." Design Automation Conference (ASP-DAC), 2010 15th Asia and South Pacific. IEEE, 2010.